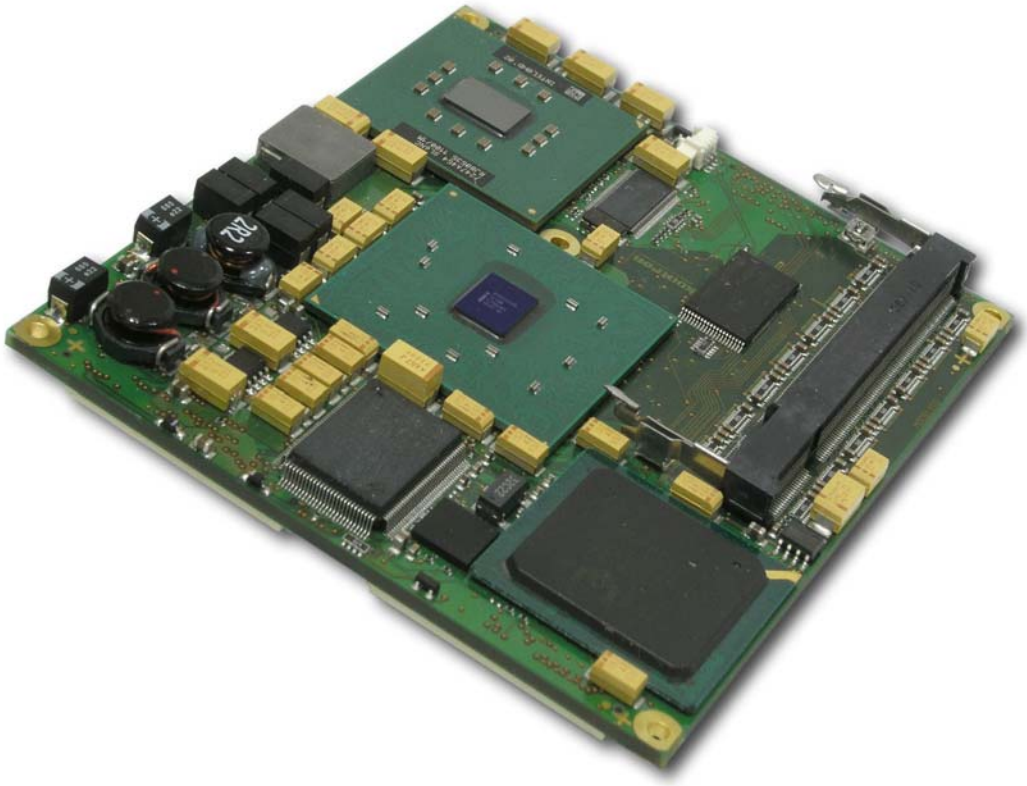

ETX Component SBC™

Specification

Document Revision 2.8

kontron

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CONTENTS

1. USER INFORMATION

1.1 *Objective*

This document is the defining specification for ETX computer modules. It specifies common mechanical and electrical characteristics for all ETX module designs to ensure physical interchangeability and electrical compatibility between modules.

1.2 *Target Audience*

This guide is intended for hardware engineers who design ETX computer modules or system baseboards for ETX computer modules.

1.3 *Assumptions*

The reader is assumed to have a hardware engineering background as well as experience with personal computer buses and peripheral interfaces. A working knowledge of practices for designs of multi-layer, printed circuit boards is assumed. Appendix A: PC Architecture Information contains suggested references for readers desiring a more extensive presentation of topics such as PCI and ISA buses and the IDE (ATAPI) interface.

1.4 *Scope*

This specification should be regarded as a supplement to industry standards that define computer buses and interfaces used on ETX modules. This specification does not include detailed information on protocols, timing, and logic levels. Please refer to the relevant industry standards for this detailed information.

ETX modules typically contain basic signal termination components such as pullup resistors. In some applications it will be necessary to place additional components on the baseboard to meet application-specific ESD, EMI, or safety requirements. These requirements vary among applications and are outside the scope of this document.

1.5 *Disclaimer*

Although the information presented in this document was carefully reviewed and is believed to be accurate, it is not guaranteed. The reader assumes all liability for the use of the information herein.

1.6 *Technical Support*

Technicians and engineers from Kontron Embedded Modules and/or its subsidiaries are available for technical support. We are committed to making our product easy to use and will help you use our products in your systems.

Before contacting Kontron Embedded Modules technical support, please consult our Web site at http://www.kontron-emea.com/emd for the latest product documentation, utilities, and drivers. If the information does not help solve the problem, contact us by telephone.

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2. INTRODUCTION

2.1 *ETX Benefits*

Embedded Technology extended (ETX) modules are very compact (~100mm square, 12mm thick), highly integrated computers. All ETX modules have a standardized form factor and a standardized connector layout that carry a specified set of signals. This standardization allows designers to create a single system "baseboard" that can accept present and future ETX modules.

ETX modules include common personal computer (PC) peripheral functions such as graphics, USB, serial, and parallel ports, keyboard/mouse, Ethernet, and IDE. The baseboard designer can optimize exactly how each of these functions is physically implemented. Connectors can be placed precisely where needed on a baseboard designed to optimally fit system packaging.

Peripheral PCI or ISA devices can be implemented directly on the baseboard rather than on mechanically unwieldy expansion cards. The ability to build a system on a single baseboard, using the computer as one "plug-in" component, simplifies packaging, eliminates cabling, and reduces system-level cost.

A single baseboard design may be used with a range of ETX modules. This flexibility can differentiate products at various price/performance points, or to design systems that have a built-in upgrade path. The modularity of an ETX solution also ensures against obsolescence as computer technology evolves. A properly designed ETX baseboard can be used with successive generations of ETX modules.

An ETX baseboard design has many of the advantages of a custom computer-board design but delivers better obsolescence protection, greatly reduces engineering effort, and achieves faster time to market.

The baseboard designer can optimize exactly how each of these functions implements physically. Designers can place connectors precisely where needed for the application on a baseboard designed to optimally fit a system's packaging.

2.2 *ETX Documentation*

This ETX Component SBC™ *Specification,* which you should read first, is one of three principal references for an ETX design. The other two references, which are available from the Kontron Embedded Modules Web site, include:

- The ETX Component SBC™ *Design Guide*, which is a general guide for baseboard design, with a focus on maximum flexibility to accommodate all ETX modules.
- Product manuals for specific ETX modules document specifications and features of each ETX module.

3. CONNECTOR PINOUT

3.1 *Connector X1*

3.1.1. PCI Bus, USB, Audio

Pin	Signal	Pin	Signal
1	GND	2	GND
3	PCICLK3	4	PCICLK4
5	GND	6	GND
7	PCICLK1	8	PCICLK2
9	REQ3#	10	GNT3#
11	GNT2#	12	3V
13	REQ2#	14	GNT1#
15	REQ1#	16	3V
17	GNT0#	18	RESERVED
19	VCC	20	VCC
21	SERIRQ	22	REQ0#
23	AD0	24	3V
25	AD1	26	AD2
27	AD4	28	AD3
29	AD6	30	AD5
31	CBE0#	32	AD7
33	AD8	34	AD9
35	GND	36	GND
37	AD10	38	AUXAL
39	AD11	40	MIC
41	AD12	42	AUXAR
43	AD13	44	ASVCC
45	AD14	46	SNDL
47	AD15	48	ASGND
49	CBE1#	50	SNDR

Pin	Signal	Pin	Signal
51	VCC	52	VCC
53	PAR	54	SERR#
55	GPERR#	56	RESERVED
57	PME#	58	USB2#
59	LOCK#	60	DEVSEL#
61	TRDY#	62	USB3#
63	IRDY#	64	STOP#
65	FRAME#	66	USB2
67	GND	68	GND
69	AD16	70	CBE2#
71	AD17	72	USB3
73	AD19	74	AD18
75	AD20	76	USB0#
77	AD22	78	AD21
79	AD23	80	USB1#
81	AD24	82	CBE3#
83	VCC	84	VCC
85	AD25	86	AD26
87	AD28	88	USB0
89	AD27	90	AD29
91	AD30	92	USB1
93	PCIRST#	94	AD31
95	INTC#	96	INTD#
97	INTA#	98	INTB#
99	GND	100	GND

3.2 *Connector X2*

3.2.1. ISA Bus

Pin	Signal	Pin	Signal
1	GND	2	GND
3	SD14	4	SD15
5	SD13	6	MASTER#
7	SD12	8	DREQ7
9	SD11	10	DACK7#
11	SD10	12	DREQ6
13	SD9	14	DACK6#
15	SD8	16	DREQ5
17	MEMW#	18	DACK5#
19	MEMR#	20	DREQ0
21	LA17	22	DACK0#
23	LA18	24	IRQ14
25	LA19	26	IRQ15
27	LA20	28	IRQ12
29	LA21	30	IRQ11
31	LA22	32	IRQ10
33	LA23	34	IO16#
35	GND	36	GND
37	SBHE#	38	M16#
39	SA0	40	OSC
41	SA1	42	BALE
43	SA2	44	TC
45	SA3	46	DACK2#
47	SA4	48	IRQ3
49	SA5	50	IRQ4

Pin	Signal	Pin	Signal
51	VCC	52	VCC
53	SA6	54	IRQ5
55	SA7	56	IRQ6
57	SA8	58	IRQ7
59	SA9	60	SYSCLK
61	SA10	62	REFSH#
63	SA11	64	DREQ1
65	SA12	66	DACK1#
67	GND	68	GND
69	SA13	70	DREQ3
71	SA14	72	DACK3#
73	SA15	74	IOR#
75	SA16	76	IOW#
77	SA18	78	SA17
79	SA19	80	SMEMR#
81	IOCHRDY	82	AEN
83	VCC	84	VCC
85	SD0	86	SMEMW#
87	SD2	88	SD1
89	SD3	90	NOWS#
91	DREQ2	92	SD4
93	SD5	94	IRQ9
95	SD6	96	SD7
97	IOCHK#	98	RSTDRV
99	GND	100	GND

3.3 *Connector X3*

3.3.1. VGA, LCD, Video, COM1, COM2, LPT/Floppy, IrDA, Mouse, Keyboard

Flat-panel Interfaces

ETX modules may implement an LVDS flat-panel interface or a parallel, digital flat-panel interface. Alternative pinouts for the two interfaces are shown in the tables below.

Pin functions for the shaded pins differ between the two flat-panel interfaces. The unshaded pins have identical functions regardless of interface type.

LVDS Interface Pinout			
Pin	**Signal**	**Pin**	**Signal**
1	GND	2	GND
3	R	4	B
5	HSY	6	G
7	VSY	8	DDCK
9	DETECT#	10	DDDA
11	LCDDO16	12	LCDDO18
13	LCDDO17	14	LCDDO19
15	GND	16	GND
17	LCDDO13	18	LCDDO15
19	LCDDO12	20	LCDDO14
21	GND	22	GND
23	LCDDO8	24	LCDDO11
25	LCDDO9	26	LCDDO10
27	GND	28	GND
29	LCDDO4	30	LCDDO7
31	LCDDO5	32	LCDDO6
33	GND	34	GND
35	LCDDO1	36	LCDDO3
37	LCDDO0	38	LCDDO2
39	VCC	40	VCC
41	JILI_DAT	42	LTGIO0
43	JILI_CLK	44	BLON#
45	BIASON	46	DIGON
47	COMP	48	Y
49	SYNC	50	C

Digital Interface Pinout			
Pin	**Signal**	**Pin**	**Signal**
1	GND	2	GND
3	R	4	B
5	HSY	6	G
7	VSY	8	DDCK
9	DETECT#	10	DDDA
11	B4	12	SHFCLK
13	B5	14	EN
15	GND	16	GND
17	B1	18	B3
19	B0	20	B2
21	GND	22	GND
23	G2	24	G5
25	G3	26	G4
27	GND	28	GND
29	R4	30	G1
31	R5	32	G0
33	GND	34	GND
35	R1	36	R3
37	R0	38	R2
39	VCC	40	VCC
41	JILI_DAT	42	VSYNC
43	JILI_CLK	44	BLON#
45	HSYNC	46	DIGON
47	COMP	48	Y
49	SYNC	50	C

Parallel Port / Floppy Interfaces

ETX parallel-port interfaces can be configured either as conventional PC parallel ports or as an interface for floppy-disk drives. The operating mode can be selected by BIOS settings or by a select pin for a specific hardware mode.

If Pin X3-51 (LPT/FLPY#) is grounded at boot time, the floppy-support mode is selected. If this pin is left floating or is held high, parallel-port mode is selected.

The mode selection is determined only at boot time. It cannot be changed until the next boot cycle.

The functions of the shaded pins differ between the parallel-port mode and the floppy-support mode. The unshaded pins are not part of the parallel port / floppy interface. These pins have identical functions regardless of the operating mode of the interface.

Parallel Port Mode Pinout			
Pin	**Signal**	**Pin**	**Signal**
51	LPT/FLPY#	52	RESERVED
53	VCC	54	GND
55	STB#	56	AFD#
57	RESERVED	58	PD7
59	IRRX	60	ERR#
61	IRTX	62	PD6
63	RXD2	64	INIT#
65	GND	66	GND
67	RTS2#	68	PD5
69	DTR2#	70	SLIN#
71	DCD2#	72	PD4
73	DSR2#	74	PD3
75	CTS2#	76	PD2
77	TXD2	78	PD1
79	RI2#	80	PD0
81	VCC	82	VCC
83	RXD1	84	ACK#
85	RTS1#	86	BUSY
87	DTR1#	88	PE
89	DCD1#	90	SLCT#
91	DSR1#	92	MSCLK
93	CTS1#	94	MSDAT
95	TXD1	96	KBCLK
97	RI1#	98	KBDAT
99	GND	100	GND

Floppy Support Mode Pinout			
Pin	**Signal**	**Pin**	**Signal**
51	LPT/FLPY#	52	RESERVED
53	VCC	54	GND
55	RESERVED	56	DENSEL
57	RESERVED	58	RESERVED
59	IRRX	60	HDSEL#
61	IRTX	62	RESERVED
63	RXD2	64	DIR#
65	GND	66	GND
67	RTS2#	68	RESERVED
69	DTR2#	70	STEP#
71	DCD2#	72	DSKCHG#
73	DSR2#	74	RDATA#
75	CTS2#	76	WP#
77	TXD2	78	TRK0#
79	RI2#	80	INDEX#
81	VCC	82	VCC
83	RXD1	84	DRV
85	RTS1#	86	MOT
87	DTR1#	88	WDATA#
89	DCD1#	90	WGATE#
91	DSR1#	92	MSCLK
93	CTS1#	94	MSDAT
95	TXD1	96	KBCLK
97	RI1#	98	KBDAT
99	GND	100	GND

3.4 *Connector X4*

3.4.1. IDE 1, IDE 2, Ethernet, Miscellaneous

Pin	Signal	Pin	Signal
1	GND	2	GND
3	5V_SB	4	PWGIN
5	PS_ON	6	SPEAKER
7	PWRBTN#	8	BATT
9	KBINH#	10	LILED#
11	RSMRST#	12	ACTLED#
13	ROMKBCS#	14	SPEEDLED#
15	EXT_PRG	16	I2CLK
17	VCC	18	VCC
19	OVCR#	20	GPCS#
21	EXTSMI#	22	I2DAT
23	SMBCLK	24	SMBDATA
25	SIDE_CS3#	26	SMBALRT#
27	SIDE_CS1#	28	DASP_S
29	SIDE_A2	30	PIDE_CS3#
31	SIDE_A0	32	PIDE_CS1#
33	GND	34	GND
35	PDIAG_S	36	PIDE_A2
37	SIDE_A1	38	PIDE_A0
39	SIDE_INTRQ	40	PIDE_A1
41	BATLOW#	42	GPE1#
43	SIDE_AK#	44	PIDE_INTRQ
45	SIDE_RDY	46	PIDE_AK#
47	SIDE_IOR#	48	PIDE_RDY
49	VCC	50	VCC

Pin	Signal	Pin	Signal
51	SIDE_IOW#	52	PIDE_IOR#
53	SIDE_DRQ	54	PIDE_IOW#
55	SIDE_D15	56	PIDE_DRQ
57	SIDE_D0	58	PIDE_D15
59	SIDE_D14	60	PIDE_D0
61	SIDE_D1	62	PIDE_D14
63	SIDE_D13	64	PIDE_D1
65	GND	66	GND
67	SIDE_D2	68	PIDE_D13
69	SIDE_D12	70	PIDE_D2
71	SIDE_D3	72	PIDE_D12
73	SIDE_D11	74	PIDE_D3
75	SIDE_D4	76	PIDE_D11
77	SIDE_D10	78	PIDE_D4
79	SIDE_D5	80	PIDE_D10
81	VCC	82	VCC
83	SIDE_D9	84	PIDE_D5
85	SIDE_D6	86	PIDE_D9
87	SIDE_D8	88	PIDE_D6
89	GPE2#	90	CBLID_P
91	RXD#	92	PIDE_D8
93	RXD	94	SIDE_D7
95	TXD#	96	PIDE_D7
97	TXD	98	HDRST#
99	GND	100	GND

4. SIGNAL DESCRIPTIONS

4.1 *Power*

4.1.1. GND

Ground. All 41 GND pins on an ETX module should be connected to the ground plane of the baseboard.

4.1.2. VCC

The baseboard provides the +5V ±5% power supply. All 21 VCC pins on an ETX module should be connected to the baseboard's +5V plane.

4.1.3. 3V

The +3.3V ±5% supply voltage is generated onboard an ETX module. These three pins may be used as a power supply for external devices. The maximum allowed external load is 500mA.

WARNING: Do not connect 3.3V pins to an external 3.3V supply.

4.2 *Reserved*

These pins are reserved for future use or for manufacturing and test purposes. Do not connect external signals to these pins.

4.3 *Connector X1*

4.3.1. PCI Signals - General

All signals are 3.3V level PCI signals. All PCI signal pullups are integrated on the ETX board and are either a 3.3V or 5V supply. For compatibility with all ETX modules, external PCI devices should have 3.3V-signal levels and be 5V tolerant. No pull-ups should be implemented externally on the PCI bus.

NOTE: For further description of PCI signals refer to Appendix A: PC Architecture Information. Refer to the *ETX Design Guide* for routing guidelines.

PCICLK1..4

PCI clock outputs for up to 4 external PCI slots or devices.

The baseboard designer should route these clocks for 1300pS total delay from the ETX connector pin to the clock pin of the PCI device. See the ETX Design Guide for typical route length calculations.

REQ[0..3]#

Bus Request signals for up to 4 external bus mastering PCI devices. When asserted, a PCI device is requesting PCI bus ownership from the arbiter.

ETX modules support varying numbers of REQ/GNT pairs. Refer to the product manual for the specific ETX module to determine how many REQ/GNT pairs are available.

GNT[0..3]#

Grant signals to PCI Masters. When asserted by the arbiter, the PCI master has been granted ownership of the PCI bus.

AD[0..31]

PCI Address and Data Bus Lines. These lines carry the address and data information for PCI transactions.

CBE[0..3]#

PCI Bus Command and Byte Enables. Bus command and byte enables are multiplexed in these lines for address and data phases, respectively.

PAR

Parity bit for the PCI bus. Generated as even parity across AD[31:0] and CBE[3:0]#.

SERR#

System Error. Asserted for hardware-error conditions such as parity errors detected in DRAM.

GPERR#

Parity Error. For PCI operation per exception granted by *PCI 2.1 Specification*.

PME#

Power-management event.

LOCK#

Lock Resource Signal. This signal indicates that either the PCI master or the bridge intends to run exclusive transfers.

DEVSEL#

Device Select. When the target device has decoded the address as its own cycle, it will assert DEVSEL#.

TRDY#

Target Ready. This signal indicates that the target is ready to complete the current data phase of a transaction.

IRDY#

Initiator Ready. This signal indicates that the initiator is ready to complete the current data phase of a transaction.

STOP#

Stop. This signal indicates that the target is requesting that the master stop the current transaction.

FRAME#

Cycle Frame of PCI Buses. This signal indicates the beginning and duration of a PCI access. The access will be either an output driven by the north bridge on behalf of the CPU, or an input during PCI master access.

PCIRST#

PCI Bus Reset. This output signal resets the entire PCI Bus. This signal is asserted during system reset.

INTA#, INTB#, INTC#, INTD#

PCI interrupts. These interrupts are sharable and are typically wired in rotation to PCI slots or devices. See the *ETX Design Guide* for details.

IDSEL

This pin is not present on the ETX module connector, but it is present on each PCI slot connector or device. IDSEL is an input to the device and is used to set a device's configuration address for PCI configuration cycles. The IDSEL pin of each device is typically connected to one of the AD lines to set a unique configuration address.

In ETX systems, the four external bus slots or devices are assumed to use AD[19..22] for IDSEL connections. See the *ETX Design Guide* for details.

4.3.2. USB Signals

USB signal-termination components are integrated on the ETX board.

In applications using external USB devices, baseboard designers will typically add USB-protection components on the baseboard, including power-supply-current limiting or fusing components.

Rout USB data signals as differential pairs. See the *ETX Design Guide* for details.

NOTE: For further description of USB signals, refer to Appendix A: PC Architecture Information.
For information regarding over-current detection on the USB, refer to signal OVCR#

USB0, USB0#

Universal Serial Bus Port 0. These are the serial data pairs for USB Port 0.
USB0 – positive signal. USB0# – negative signal.

USB1, USB1#

Universal Serial Bus Port 1. These are the serial data pairs for USB Port 1.
USB1 – positive signal. USB1# – negative signal.

USB2, USB2#

Universal Serial Bus Port 2. These are the serial data pairs for USB Port 2.
USB2 – positive signal. USB2# – negative signal.

USB3, USB3#

Universal Serial Bus Port 3. These are the serial data pairs for USB Port 3.
USB3 – positive signal. USB3# – negative signal.

4.3.3. Audio Signals

SNDL/ SNDR

Line-level stereo output left/ right. These outputs have a nominal level of 1 volt RMS into a 10K-impedance load. These outputs cannot drive low-impedance speakers directly. See the *ETX Design Guide* for typical amplifier circuits.

AUXAL/ AUXAR

Auxiliary A input left/ right. This signal connects to an internal or external CD-ROM analog output or a similar line-level audio source. Minimum input impedance is 5KOhm. Nominal input level is 1 volt RMS.

MIC

Microphone input. Minimum input impedance is 5KOhm, max. input voltage is 0.15 V_{p-p}.

ASGND

Analog ground for sound controller. Use this signal ground for an external amplifier to achieve lowest audio-noise levels.

ASVCC

Analog supply voltage for sound controller. This output is used only for production test. Do not make external connections to this pin.

4.3.4. Miscellaneous

SERIRQ

Serial interrupt request. This pin supports the serial-interrupt protocol.

NOTE: Refer to the ETX product manual for information on the support of this signal.

4.4 *Connector X2*

4.4.1. ISA Signals

All required signal pullups are integrated into the ETX module. In some applications, it may be desirable to add additional signal-termination components to the baseboard.

NOTE: For further description of ISA signals, refer to the Appendix A: PC Architecture Information.

SD[0..15]

These signals provide data bus bits 0 to 15 for peripheral devices. All 8-bit devices use SD0[0..7] for data transfers. All 16-bit devices use SD[0..15].

To support 8-bit devices, the data on SD[8..15] is gated to SD[0..7] during 8-bit transfers to these devices. All 16-bit CPU cycles automatically convert to two, 8-bit cycles for 8-bit peripherals.

SA[0..19]

Address bits 0 through 15 are used to address I/O devices. Address bits 0 through 19 are used to address memory within the system. These 20 address lines, in addition to LA[17..23], allow access of up to 16MB of memory. SA[0..19] are gated on the ISA bus when BALE is high and latched on to the falling edge of BALE.

SBHE#

Bus High Enable indicates a data transfer on the upper byte of the data bus SD[8..15]. All 16-bit I/O devices use SBHE# to enable data-bus buffers on SD[8..15].

BALE

BALE is an active-high pulse generated at the beginning of a bus cycle initiated by a CPU module. It indicates when the SA[0..19], LA17.23, AEN, and SBHE# signals are valid.

AEN

AEN is an active-high output that indicates a DMA transfer cycle. Only resources with a active DACK# signal should respond to the command lines when AEN is high.

MEMR#

MEMR# instructs memory devices to drive data onto the data bus. MEMR# is active for all memory-read cycles.

SMEMR#

SMEMR# instructs memory devices to drive data onto the data bus. SMEMR# is active for memory-read cycles to addresses below 1MB.

MEMW#

MEMW# instructs memory devices to store the data present on the data bus. MEMW# is active for all memory-write cycles.

SMEMW#

SMEMW# instructs memory devices to store the data present on the data bus. SMEMW# is active for all memory-write cycles to address below 1MB.

IOR#

I/O read instructs an I/O device to drive its data onto the data bus. It may be driven by the CPU or by the DMA controller. IOR# is inactive (high) during refresh cycles.

IOW#

I/O write instructs an I/O device to store the data present on the data bus. It may be driven by the CPU or by the DMA controller. IOW# is inactive (high) during refresh cycles.

IOCHK#

IOCHK# is an active-low input signal that indicates that an error has occurred on the module bus. If I/O checking is enabled on the CPU module, an IOCHK# assertion by a peripheral device sends a NMI to the processor.

IOCHRDY

The I/O Channel Ready is pulled low to extend the read or write cycles of any bus access when required. The CPU, DMA controllers or refresh controller can initiate the cycle. A peripheral that cannot present read data or strobe in write data within this amount of time uses IOCHRDY to extend these cycles.

This signal should not be held low for more than 2.5 µs for normal operation. Any extension to more than 2.5 µs does not guarantee proper DRAM memory content because memory refresh is disabled when IOCHRDY is low.

M16#

The M16# signal determines when a 16-bit to 8-bit conversion is needed for memory bus cycles. A conversion is done any time the CPU module requests a 16-bit memory cycle while the M16# line is high. If M16# is high, 16-bit CPU cycles are automatically converted on the bus into two 8-bit cycles. If M16# is low, an access to peripherals is done 16-bits wide.

IO16#

The IO16# signal determines when a 16-bit to 8-bit conversion is needed for I/O bus cycles. A conversion is done any time the CPU module requests a 16-bit I/O cycle while the IO16# line is high. If IO16# is high, 16-bit CPU cycles are automatically converted on the bus into two 8-bit cycles. If IO16# is low, an access to peripherals is done at 16-bit width.

REFSH#

REFSH# is pulled low whenever a refresh cycle is initiated. A refresh cycle is activated every 15.6 us to prevent loss of DRAM data.

NOWS#

The Zero wait-state signal tells the CPU to complete the current bus cycle without inserting the default wait states. By default, the CPU inserts 4 wait states for 8-bit transfers and 1 wait state for 16-bit transfers.

MASTER#

This signal is used with a DRQ line to gain control of the system bus. A processor or a DMA controller on the I/O channel may issue a DRQ to a DMA channel in cascade mode and receive a DACK#. Upon receiving the DACK#, a bus master may pull MASTER# low, which will allow it to control the system address, data, and control lines. After MASTER# is low, the bus master must wait one system clock period before driving the address and data lines and two clock periods before issuing a read or write command. If this signal is held low for more than 15 us, system memory may be lost as memory refresh is disabled during this process.

SYSCLK

SYSCLK is supplied by the CPU module and has a nominal frequency of about 8 MHz with a duty cycle of 40-60 percent. The frequency supplied by different CPU modules may vary. This signal is supplied at all times except when the CPU module is in sleep mode.

OSC

The CPU module supplies OSC. It has a nominal frequency of 14.31818 MHz and a duty cycle of 40-60 percent. This signal is supplied at all times except when the CPU module is in sleep mode.

RESETDRV

This active-high output is system reset generated from CPU modules. It is responsible for resetting external devices.

DREQ[0, 1, 2, 3, 5, 6, 7]

The asynchronous DMA request inputs are used by external devices to indicate when they need service from the CPU module's DAM controllers. DREQ0..3 are used for transfers between 8-bit I/O adapters and system memory. DREQ5..7 are used for transfers between 16-bit I/O adapters and system memory. DRQ4 is not available externally. All DRQ pins have pullup resistors on CPU modules.

DACK[0, 1, 2, 3, 5, 6, 7]#

DMA acknowledge 0..3 and 5.7 acknowledge DMA requests. They are active-low.

TC

The active-high output TC indicates that one of the DMA channels has transferred all data.

IRQ[3..7, 9,15]

These are the asynchronous interrupt request lines. IRQ0, 1, 2 and 8 are not available as external interrupts because they are used internally on the CPU module. All IRQ signals are inactive-high. The interrupt requests are prioritized. IRQ9 through IRQ12 and IRQ14 through IRQ15 have the highest priority (IRQ9 is the highest). IRQ3 through IRQ7 have the lowest priority (IRQ7 is the lowest). An interrupt request is generated when an IRQ line is raised from low to high. The line must be held high until the CPU acknowledges the interrupt request (interrupt-service routine).

4.5 *Connector X3*

4.5.1. VGA Signals

External termination components are required on the VGA analog video outputs. See the *ETX Design Guide* for details.

NOTE: For further description of VGA signals, refer to Appendix A: PC Architecture Information.

HSY

Horizontal Sync: This output supplies the horizontal synchronization pulse to the CRT monitor.

VSY

Vertical Sync: This output supplies the vertical synchronization pulse to the CRT monitor.

R, G, B

Red, green and blue analog video output signals for CRT monitors. These lines should be terminated with 75 ohms to ground at the video connector.

DDCK, DDDA

These two pins can be used for a DDC interface between the graphics-controller chip and the CRT monitor.

4.5.2. LVDS Flat-Panel Interface Signals

NOTE: ETX modules may implement either this LVDS flat-panel interface or the digital interface described in section 4.5.3. Refer to the specific ETX module product manual for additional information.

LCDDO[0..19]

LCD data output pins for LVDS support. These signals are differential and should be routed as differential pairs. See the *ETX Design Guide* for more information.

An ETX module that supports LVDS output must implement at least LCDDO[0..7]. These four signal pairs can support a single channel TFT interface of 18 bits or less.

The implementation of LCDDO[8..19] is optional. Refer to the specific ETX product manual for information about the implementation of these signals.

Single channel LVDS links use the first channel only. Dual channel links, which are commonly used to transmit high data rates, will use both the first and second channels.

The Txout3 and Txout3# signals are used only for 24-bit LCD panels. ETX modules that do not support 24-bit panels will not implement LCDDO[8..9] or LCCDO[18..19].

Pin Name	LVDS Signal	Channel
LCDDO0	Txout0#	first
LCDDO1	Txout0	first
LCDDO2	Txout1#	first
LCDDO3	Txout1	first
LCDDO4	Txout2#	first
LCDDO5	Txout2	first
LCDDO6	Txclk#	first
LCDDO7	Txclk	first
LCDDO8	Txout3#	first
LCDDO9	Txout3	first
LCDDO10	Txout0#	second
LCDDO11	Txout0	second
LCDDO12	Txout1#	second
LCDDO13	Txout1	second
LCDDO14	Txout2#	second
LCDDO15	Txout2	second
LCDDO16	Txclk#	second
LCDDO17	Txclk	second
LCDDO18	Txout3#	second
LCDDO19	Txout3	second

BIASON

Controls contrast voltage to the panel.

DIGON

Controls digital power to the panel.

BLON#

Controls backlight power to the panel.

LTGIO0

General purpose I/O pin; it is not used by the JILI interface.

JILI_CLK, JILI_DAT

I^2C interface for panel parameter EEPROM. This EEPROM is mounted on JILI adapter. The data in the EEPROM allows the ETX module to automatically set the proper timing parameters for a specific LCD panel. These lines are pulled up to 3.3 volts on the ETX module. Power the EEPROM with 3.3 volts.

DETECT#

Panel hot-plug detection. Implementation of this pin is optional. See the specific ETX module product manual for details.

4.5.3. Digital Flat-Panel Interface Signals

NOTE: ETX modules may implement either this parallel interface or the LVDS flat-panel interface described in section 4.5.2. Refer to the specific ETX module product manual for additional information.

R[0..5], G[0..5], B[0..5]

Parallel digital signals for red, green, and blue pixel data.

HSYNC

Horizontal Sync: This output supplies the horizontal-synchronization pulse for flat panels. This signal is named LP (Line Pulse) in some flat-panel literature.

VSYNC

Vertical Sync: This output supplies the vertical-synchronization pulse for flat panels. This signal is named FLM (First Line Marker) in some flat-panel literature.

DE

Data-enable signal. Usage depends on display type.

SHCLK

This signal is for the panel's data clock.

DETECT#

Panel hot-plug detection. Implementation of this pin is optional. See the manual for the specific ETX module product for details.

NOTE: Refer to your ETX product manual for display wiring information.

4.5.4. Television Output Signals

External termination components are required on analog television outputs. See the *ETX Design Guide* for details.

NOTE: Television output is not a standard ETX feature. Refer to your ETX product manual for additional information.

SYNC

Composite Sync for RGB Video (SCART).

Y

Analog Output: outputs either Y (Luminance) for S-Video, or Red for RGB Video (SCART).

C

Analog Output: outputs either C (Color/Chrominance) for S-Video, or Green for RGB Video.

COMP

Analog Output: outputs either Composite Video, or Blue for RGB Video.

4.5.5. Serial Port Signals

Signals for serial ports on the ETX module connectors are logic-level signals. External transceiver devices are necessary for the conversion of the logic-level signals to the desired physical interface such as RS232, RS422, or RS485. See the *ETX Design Guide* for details.

DTR1#, DTR2#

Active-low data terminal ready outputs for the serial port. The handshake output signal notifies the modem that the UART is ready to establish a data-communication link.

RI1#, RI2#

Active-low input is for the serial port. Handshake signals notify the UART when a telephone-ring signal is detected by the modem.

TXD1, TXD2

Transmitter serial-data output from serial port.

RXD1, RXD2

Receiver serial-data input.

CTS1#, CTS2#

Active-low input for serial ports. Handshake signals notify the UART when the modem is ready to receive data.

RTS1#, RTS2#

Active-low output for serial port. Handshake signals notify the modem when the UART is ready to transmit data.

DCD1#, DCD2#

Active-low input for serial port. Handshake signals notify the UART when a carrier signal is detected by the modem.

DSR1#, DSR2#

This active-low input is for serial port. Handshake signals are use to notify the UART that the modem is ready to establish the communication link.

4.5.6. PS/2 Keyboard, PS/2 Mouse Signals

KBDAT

Bi-directional keyboard-data signal.

KBCLK

Keyboard-clock signal.

MSDAT

Bi-directional mouse-data signal.

MSCLK

Mouse-clock signal.

4.5.7. IRDA (SIR) Signals

IRTX, IRRX

Infrared transmit and receive pins.

4.6 *Parallel Port Signals*

Signals for the parallel port require external termination components. See the *ETX Design Guide* for details.

The parallel port has two alternative operating modes: parallel port and floppy disk. If the parallel port is used in parallel-port mode, floppy-disk support is not available via the parallel port. The LPT/FLPY# pin, which switches the parallel-port modes, is sensed only at boot and cannot be changed dynamically.

If simultaneous floppy drive and parallel support is needed, an external floppy controller may be incorporated into the baseboard design.

LPT/FLPY#

This ETX input signal selects whether parallel-port pins will implement parallel port or floppy support functionality. There is an internal pullup on this signal. If this signal is high or unconnected, the following parallel-port pin functions are in effect:

STB#

This active-low signal strobes the printer data into the printer.

AFD#

This active-low output tells the printer to automatically feed the next single line after each preceding line has been printed.

PD[0..7]

This bi-directional parallel data bus transfers information between the CPU and peripherals.

ERR#

This active-low signal indicates an error has occurred with the printer.

INIT#

This active-low signal initiates the printer when low.

SLIN#

This active-low signal selects the printer.

ACK#

This active-low output from the printer indicates that it has received the previous data and that it is ready to receive new data.

BUSY

This signal indicates that the printer is busy and not ready to receive new data.

PE

This signal indicates that the printer is out of paper.

SLCT#

This active-high output from the printer indicates that its power is on.

4.6.1. Floppy Signals

ETX modules support only a single floppy drive over the parallel-port interface. When operating in floppy-disk mode, the parallel port is not available.

LPT/FLPY#

This ETX input signal selects whether the parallel-port pins will implement parallel port or floppy-support functionality. There is an internal pullup on this signal. If this signal is low, the following floppy-support functions are supported over the parallel-port pins.

DENSEL

Indicates whether a low (250/300Kb/s) or high (500/1000Kbs) data rate has been selected.

INDEX#

This active-low Schmitt Trigger input signal is asserted by the disk drive when the diskette index hole is sensed.

TRK0#

This active-low Schmitt Trigger input signal is asserted by the disk drive when the head is positioned over the outermost track.

WP#

This active-low Schmitt Trigger input signal is asserted by the disk drive when a disk is write-protected.

RDATA#

The active-low, raw-data read signal from the disk drive. Each falling edge represents a flux transition of the encoded data.

DSKCHG#

This active-low input signal is asserted by the disk drive when the drive door has been opened.

DRV

This signal selects the floppy drive.

MOT

This active-low output activates the disk-drive motor.

HDSEL#

This active-low output determines which disk-drive head is active.
Low = Head 0. High (open) = Head 1.

DIR#

This active-low output determines the direction of head movement.
Low = step-in. High (open) = step-out.

STEP#

This active-low output signal is pulsed at a software-programmable rate to move the head during a seek operation.

WDATA#

This active-low output is a write precompensated serial-data stream to be written onto the selected disk drive. Each falling edge causes a flux change on the media.

WGATE#

This active-low output enables the write circuitry of the selected disk drive.

4.7 *Connector X4*

4.7.1. IDE Signals

IDE signals are duplicated for primary and secondary IDE channels. For each signal, the first signal name is for the primary channel and the second signal name is for the secondary channel.

PIDE_D0..15/ SIDE_D0..15

IDE Data Bus.

PIDE_A[0..2]/ SIDE_A[0..2]

IDE Address Bus.

PIDE_CS1#/ SIDE_CS1#

IDE Chip Select 1. This is the Chip Select 1 command output pin that enables the IDE device to watch the Read/Write Command.

PIDE_CS3#/ SIDE_CS3#

IDE Chip Select 3. This is the Chip Select 3 command output pin that enables the IDE device to watch the Read/Write Command.

PIDE_DRQ/ SIDE_DRQ

IDE DMA Request for IDE Master. This signal is asserted by an IDE device. It will be active-high in DMA or Ultra-33 mode and always be inactive-low in PIO mode.

PIDED_AK#/ SIDED_AK#

IDE DACK# for IDE Master. This signal grants the IDE DMA request to begin the IDE Master Transfer in DMA or Ultra-33 mode.

PIDE_RDY/ SIDE_RDY

IDE Ready. This is the input pin from the IDE Channel. It indicates that the IDE device is ready to terminate the IDE command in PIO mode. The IDE device can de-assert this input to expand the IDE command if the device is not ready. In Ultra-33 mode, this pin has different functions. See the references for details.

PIDE_IOR#/ SIDE_IOR#

IDE IOR# Command. This IOR# command output pin tells the IDE device to assert the Read Data in PIO and DMA mode. In Ultra-33 mode, this pin has different functions.

PIDE_IOW#/ SIDE_IOW#

IDE IOW# Command. This IOW# command output pin notifies the IDE device that the available Write Data is already asserted by the IDE Busmaster in PIO and DMA mode. In Ultra-33 mode, this pin has different functions.

PIDE_INTRQ/ SIDE_INTRQ

Interrupt-request signal from the IDE device.

HDRST#

Low-active hardware reset (RSTDRV inverted).

DASP_S

Time-multiplexed, open-collector output that indicates that a drive is active. It is also used for Master/Slave negotiation on the secondary IDE channel.

If an IDE device such as a Flash Disk exists onboard the ETX module, this signal must be connected to the DASP_S pin of any other device connected to the secondary IDE channel.

NOTE: Refer to your ETX module product manual for additional information.

PDIAG_S

The signal is used for Master/Slave negotiation on the secondary IDE channel. It is asserted by the Slave to indicate to a master that the slave has passed its internal diagnostic command.

If an IDE device such as a Flash Disk exists onboard the ETX module, this signal must be connected to the PDIAG_S pin of any other device connected to the secondary IDE channel.

On ETX modules that support DMA66 or DMA100, this pin may also detect the presence of the 80-conductor IDE cable that is needed to support these modes.

NOTE: Refer to your ETX module product manual for additional information.

CBLID_P

On ETX modules that support DMA66 or DMA100, this pin may be used to detect the presence of an 80-conductor IDE cable on the primary IDE channel. This allows BIOS or system software to determine whether to enable high-speed transfer modes.

NOTE: Refer to your ETX module product manual for additional information.

4.7.2. Ethernet Signals

The ETX Ethernet interface is designed for use with an external 1:1/ 1:1 transformer. See the transformer specification below.

NOTE: Refer to the *ETX Design Guide* for more information on the Ethernet interface and for routing guidelines for Ethernet signals.

TXD#, TXD (Analog Twisted Pair)

Ethernet Transmit Differential Pair. These pins transmit the serial-bit stream on the Unshielded Twisted Pair (UTP) cable. The current-driven differential driver can be two-level (10BASE-T) or three-level (100BASE-TX) signals, depending on the mode of operation. These signals interface to the Ethernet cable through an isolation transformer.

RXD#, RXD (Analog Twisted Pair)

Ethernet Receive Differential Pair. These pins receive the serial-bit stream from the isolation transformer. The bit stream can be transmitted in either two-level (10BASE-T) or three-level (100BASE-TX) signals, depending on the mode of operation. These signals interface to the Ethernet cable through an isolation transformer.

ACTLED#

The Activity LED pin indicates either transmitted or received data activity on the Ethernet port. This pin is asserted low when activity is detected. It can sink 5mA to ground through an external LED and a limiting resistor to a 3.3V source.

LILED#

The Link Integrity LED pin indicates link integrity. This pin is asserted low when the link is valid. It can sink 5mA to ground through an external LED and a limiting resistor to a 3.3V source.

SPEEDLED#

The Speed LED pin indicates high-speed operation. This LED is not supported by all ETX boards. This pin is asserted low when a 100Mbps link is detected and is not asserted for a

10Mbps link. It can sink 5mA to ground through an external LED and a limiting resistor to a 3.3V source.

Ethernet Transformer Specification	
Turns ratio transmit:	1:1 +/- 5%
Turns ratio receive:	1:1 +/- 5%
Insertion Loss 1 to 60 MHz:	max. 1 dB
Return Loss 1 to 80 MHz:	max. 10 dB
Common Mode Rejection	
30 to 100 MHz:	max. 30 dB
100 to 500 MHz:	max. 20 dB
Cross Talk 1 to 80 MHz:	max. 35 dB
Hi-Pot (Pri-Sec):	min. 1500VRMS

Supported Ethernet Transformer Examples
Pulse H0002
Pulse H1012T
Valor MD6301NDS1
Valor ST6118T
Bel Fuse S558-5999-46
Delta Electronics LF8200M

4.7.3. Power Control Signals

PWGIN

An active-high input to the ETX from an external power supply indicates that the power is good and that the ETX can begin booting. Use of this signal is not required because the ETX module contains its own power-good logic.

The PWGIN signal also can be used as an active-low reset input to the ETX module.

5V_SB

Power input for the internal suspend and power-control circuitry. Connect to a 5V, 100mA stand-by power source available. This can be a no-connect if a standby supply is unavailable.

PS_ON

Active-low output from ETX module. It can be connected to the PS_ON input of an ATX power supply to switch the main output. For this pin to function, 5V_SB must be supplied to the ETX module.

PWRBTN#

Power Button Input. Connect to GND with momentary-contact switch or open-collector driver to implement ATX power-button control of PS_ON. For this pin to function, 5V_SB must be supplied to the ETX module.

4.7.4. Power-Management Signals

NOTE: Support of these signals is not required by the ETX specification. Refer to the specific ETX product manual for information about supported power management signals.

For these pins to function while VCC is powered down, 5V_SB must be supplied to the ETX module.

Rhese signals generally have pullup resistors to the suspend power supply inside the ETX module. Care must be taken in interfacing these signals to logic that is powered down when 5V_SB is active.

RSMRST#

Resume Reset input. This input may be driven low by external circuitry to reset the power-management logic on the ETX module.

SMBALRT#

System Management Bus Alert input. This signal may be driven low by SMB devices to signal an event on the SM Bus.

BATLOW#

Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low, or may be used to signal some other external power-management event.

GPE1#

General-purpose, power-management event input 1. This may be driven low by external circuitry to signal an external power-management event. Within the ETX module, this pin is commonly connected to the chipset's LID# input.

GPE2#

General-purpose, power-management event input 2. This may be driven low by external circuitry to signal an external power-management event. Within the ETX module, this pin is commonly connected to the chipset's RING# input.

EXTSMI

System-management-interrupt input. This may be driven low by external circuitry to initiate an SMI.

4.7.5. Miscellaneous Signals

SPEAKER

PC speaker output signal. This logic-level signal can be connected to an external transistor to drive a piezoelectric or dynamic speaker.

NOTE: Refer to the *ETX Design Guide* for more information.

BATT

This is a 3V-backup-cell input. BATT is typically connected to a 3V-lithium-backup cell for RTC operation and CMOS register non-volatility in the absence of system power.

When RTC operation is not required by the application, some ETX modules can back up CMOS contents to EEPROM without using a battery.

NOTE: Refer to your ETX module product manual for RTC current requirements.

I^2CLK, I^2DAT

These clock and data lines implement an I^2C-bus, which supports external slave devices only. Data rate is approximate 1-10kHz. This interface supports EEPROMs and other simple I/O-devices

NOTE: Refer to your ETX product manual for additional information.

SMBDATA, SMBCLK

System Management Bus clock and data lines. This may be used to support external SMBUS devices such as temperature and battery monitoring chips. The addresses of external SMBUS devices must be chosen so they do not conflict with addresses used internally on the ETX module. Implementation of these pins is optional. See the specific ETX module product manual for details

NOTE: Refer to your ETX product manual for additional information.

KBINH#

Keyboard Inhibit. Asserting this pin disables data input from the keyboard. This is not supported on all ETX modules.

OVCR#

Over-current detect input. This signal monitors the USB power over-current. Pull with open collector to GND if over-current is detected.

ROMKBCS#, EXT_PRG

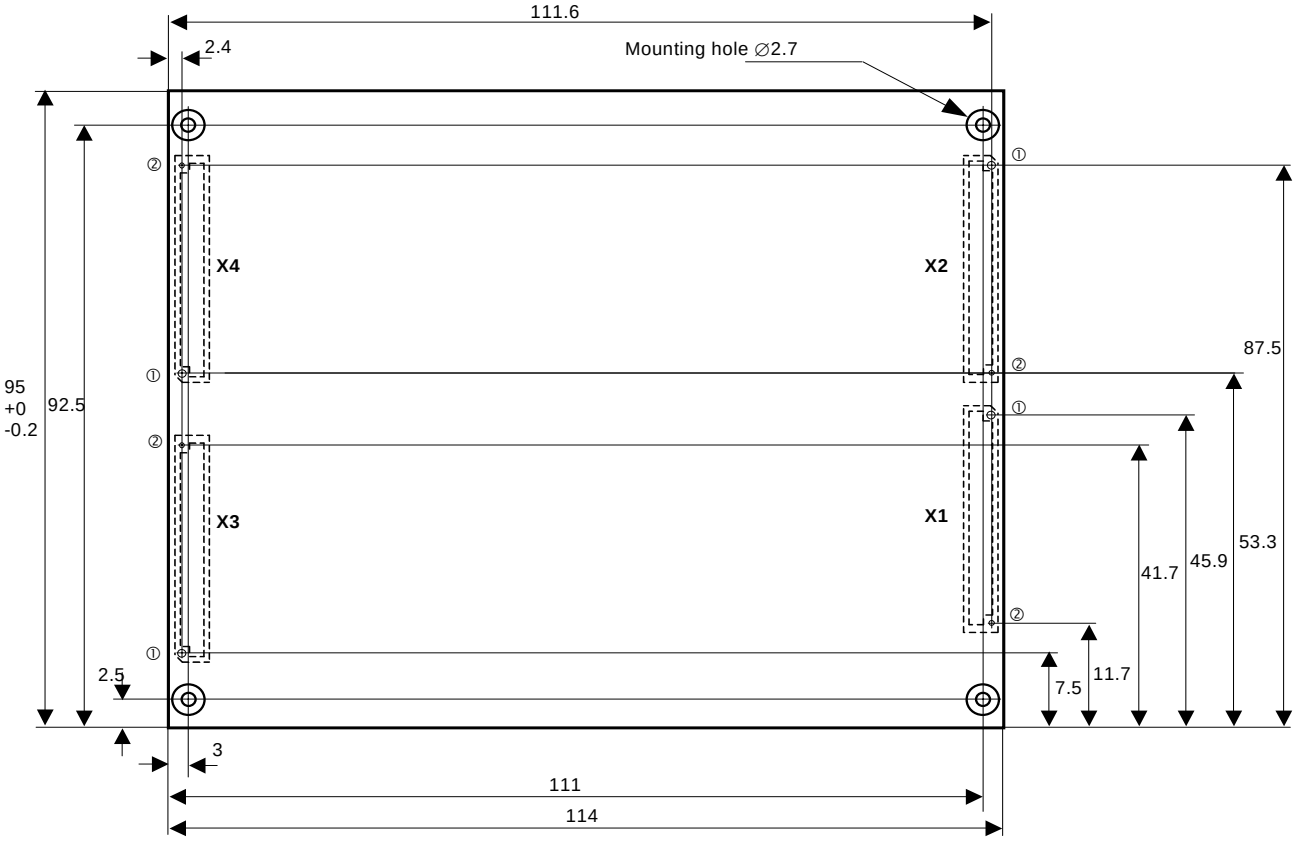
Reserved. Do not connect to this pin.

GPCS#

Reserved. Some modules may use this pin as an active-low programmable chip select signal or for some other module-specific functions. See product manual for documentation.

5. MECHANICAL CHARACTERISTICS

5.1 *Dimensions of ETX Component SBC™*



CAUTION: DO NOT USE THIS DRAWING FOR BASEBOARD LAYOUT. (SEE SECTION 5.5).

Notes: The height (Y) dimension is 100mm (instead of 95mm) on some ETX Component SBCs. This does not change the relative location of the connectors and mounting holes. The 100mm height modules are interchangeable with 95mm modules.

An ETX module, including the heat-spreader plate, has a maximum thickness of approximately 12mm. The top components are up to 8mm high, and the bottom components are up to 2mm high. Headers X1 to X4 (FX8-100P-SV) on ETX are 2.8mm high and connect to the corresponding receptacles on the baseboard. See Section 5.3 for baseboard-receptacle specifications.

5.2 *Heat Spreader and Heat-sink Considerations*

The heat-spreader is a 2mm-thick aluminum plate. It provides a thermal-interface surface for heat removal from the ETX module. Because of the thickness of the plate, components, which must fit under the plate, are limited to a height of 6mm unless clearance holes are provided.

Clearance holes in the heat-spreader plate are permitted for user access such as SODIMM removal or to allow the use of high-profile components up to 8mm high. All hole locations and sizes should be carefully considered so that the mechanical integrity of the heat-spreader is maintained.

The heat-spreader is thermally coupled to the CPU die or package surface, and it may also be coupled to other heat-generating devices on the module. The heat-spreader is the thermal-interface surface for most of the heat generated within the module. The heat spreader is not intended as a heat sink, although it may be suitable for this purpose on low-power modules operating under benign conditions. Higher power modules or higher temperature conditions will require heat-removal devices (such as heat sinks with fans and heat pipes) to be attached to the heat-spreader, or they may need to be thermally coupled to a chassis.

Thermal dissipation varies considerably among ETX modules and proper heat removal from the heat-spreader plate is an essential consideration for any ETX design. For maximum flexibility, ETX cooling methods should couple to as much of the heat-spreader plate area as possible because the location of the CPU varies with each ETX module design.

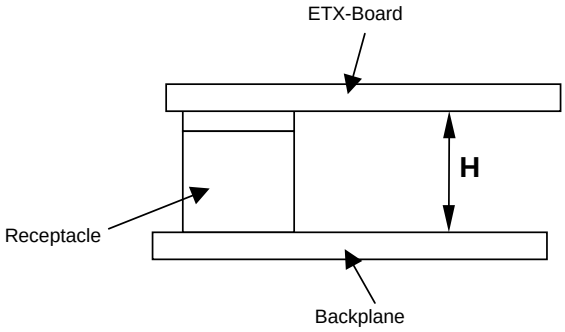
NOTE: Refer to your ETX module product manual for the exact definition of the heat-spreader and cooling requirements and operating temperature limits for that module

5.3 *Specifications Baseboard Connector and Standoffs*

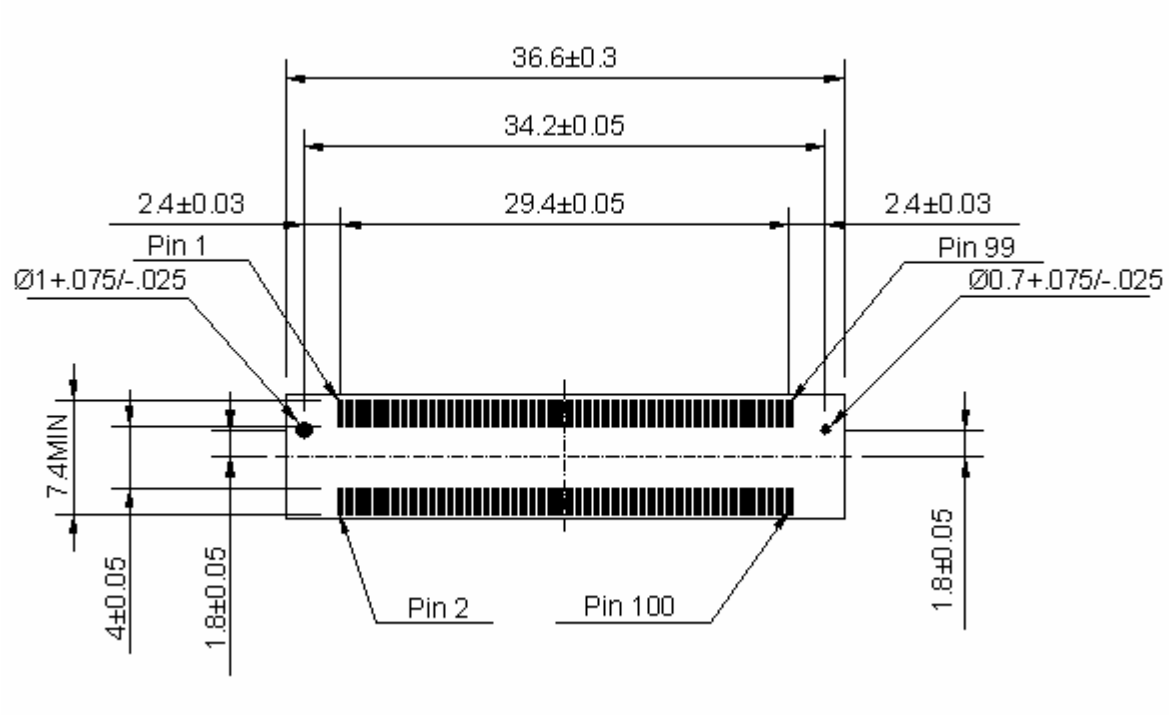
To achieve various stacking heights, the receptacles for ETX baseboards are available in two heights.

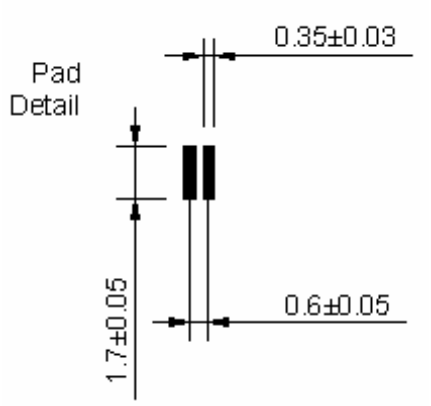
Manufacturer	Order number	Resulting Height H between Backplane and ETX Board	Standoff Specification
HIROSE	FX8-100S-SV	3.0mm	3.0mm ±0.2mm
	FX8C-100S-SV5	9.5mm	9.5mm+0.0 -0.1mm

Parameter	Hirose FX8 Series
Current Capacity	0.4A per pin
Rated voltage	100V AC
Insulation resistance	100MΩ or greater @ 250V DC
Withstand voltage	300V AC r.m.s.
Contact resistance	45mΩ or less @ 100mA DC
Insulation	PPS resin (Light brown, UL94V-0)
Contacts	Phosphor bronze (Contacts and leads-gold plating)

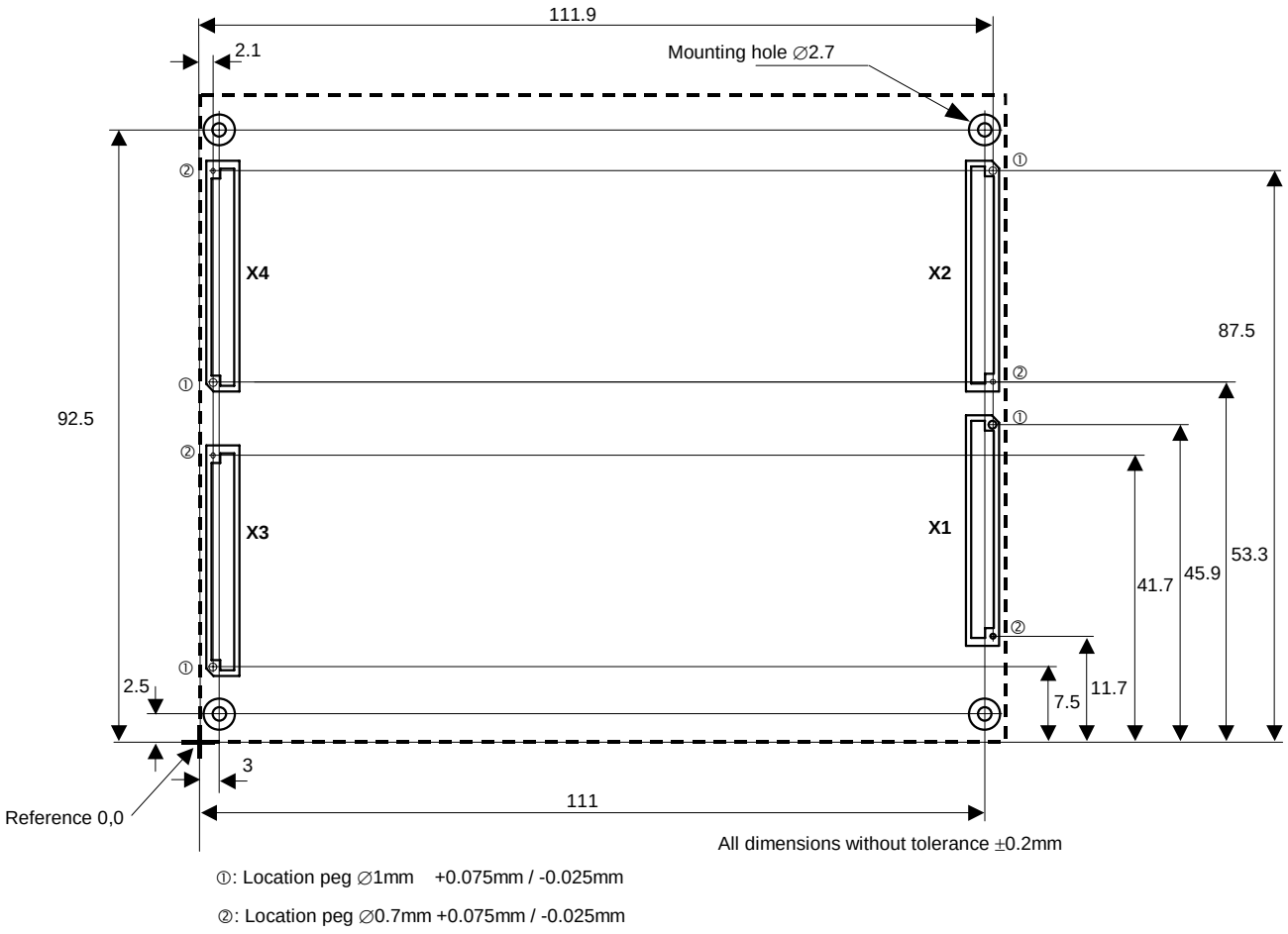


5.4 *PCB Footprint of Receptacle FX8-100S*





5.5 *Backplane Layout*



The outline shown here is for modules with a Y dimension of 95mm. To accommodate both 95mm and 100mm ETX modules, the 95mm outline shown here should be expanded by 2.5mm on the top and 2.5mm on the bottom.

The relative mounting hole and connector locations on the 95mm and 100mm modules are the same, only the Y envelope dimension varies. A given baseboard design can accommodate both 95mm and 100mm modules provided sufficient clearance is allowed for the 100mm module.

6. APPENDIX A: PC ARCHITECTURE INFORMATION

The following sources of information can help you better understand PC architecture.

6.1 *General PC Architecture*

- *Embedded PCs*, Markt&Technik GmbH, ISBN 3-8272-5314-4 (German)
- *Hardware Bible*, Winn L. Rosch, SAMS, 1997, 0-672-30954-8
- *Interfacing to the IBM Personal Computer*, Second Edition, Lewis C. Eggebrecht, SAMS, 1990, ISBN 0-672-22722-3
- *The Indispensable PC Hardware Book*, Hans-Peter Messmer, Addison-Wesley, 1994, ISBN 0-201-62424-9
- *The PC Handbook: For Engineers, Programmers, and Other Serious PC Users, Sixth Edition*, John P. Choisser and John O. Foster, Annabooks, 1997, ISBN 0-929392-36-1

6.2 *Buses*

6.2.1. ISA, Standard PS/2 – Connectors

- AT Bus Design: Eight and Sixteen-Bit ISA, E-ISA and EISA Design, Edward Solari, Annabooks, 1990, ISBN 0-929392-08-6
- AT IBM Technical Reference Vol 1&2, 1985
- ISA & EISA Theory and Operation, Edward Solari, Annabooks, 1992, ISBN 0929392159
- ISA Bus Specifications and Application Notes, Jan. 30, 1990, Intel
- ISA System Architecture, Third Edition, Tom Shanley and Don Anderson, Addison-Wesley Publishing Company, 1995, ISBN 0-201-40996-8
- Personal Computer Bus Standard P996, Draft D2.00, Jan. 18, 1990, IEEE Inc
- Technical Reference Guide, Extended Industry Standard Architecture Expansion Bus, Compaq 1989

6.2.2. PCI/104

- Embedded PC 104 Consortium
  The consortium provides information about PC/104 and PC/104-Plus technology. You can search for information about the consortium on the Web.

- PCI SIG
  The PCI-SIG provides a forum for its ~900 member companies, who develop PCI products based on the specifications that are created by the PCI-SIG. You can search for information about the SIG on the Web.

- *PCI & PCI-X Hardware and Software Architecture & Design*, Fifth Edition, Edward Solari and George Willse, Annabooks, 2001, ISBN 0-929392-63-9.

- *PCI System Architecture,* Tom Shanley and Don Anderson, Addison-Wesley, 2000, ISBN 0-201-30974-2.

6.3 *Ports*

6.3.1. RS-232 Serial

- EIA-232-E standard
  The EIA-232-E standard specifies the interface between (for example) a modem and a computer so that they can exchange data. The computer can then send data to the modem, which then sends the data over a telephone line. The data that the modem receives from the telephone line can then be sent to the computer. You can search for information about the standard on the Web.

- *RS-232 Made Easy: Connecting Computers, Printers, Terminals, and Modems*, Martin D. Seyer, Prentice Hall, 1991, ISBN 0-13-749854-3

- National Semiconductor
  The Interface Data Book includes application notes. Type “232” as search criteria to obtain a list of application notes. You can search for information about the data book on National Semiconductor’s Web site.

6.3.2. Serial ATA

Serial AT Attachment (ATA) Working Group
This X3T10 standard defines an integrated bus interface between disk drives and host processors. It provides a common point of attachment for systems manufacturers and the system. You can search for information about the working group on the Web.
We recommend you also search the Web for information on *4.2 I/O cable*, if you use hard disks in a DMA3 or PIO4 mode.

6.3.3. USB

USB Specification
USB Implementers Forum, Inc. is a non-profit corporation founded by the group of companies that developed the Universal Serial Bus specification. The USB-IF was formed to provide a support organization and forum for the advancement and adoption of Universal Serial Bus technology. You can search for information about the standard on the Web.

6.4 *Programming*

- *C Programmer's Guide to Serial Communications*, Second Edition, Joe Campbell, SAMS, 1987, ISBN 0-672-22584-0
- *Programmer's Guide to the EGA, VGA, and Super VGA Cards*, Third Edition, Richard Ferraro, Addison-Wesley, 1990, ISBN 0-201-57025-4
- *The Programmer's PC Sourcebook,* Second Edition, Thom Hogan, Microsoft Press, 1991, ISBN 1-55615-321-X
- *Undocumented PC, A Programmer's Guide to I/O, CPUs, and Fixed Memory Areas*, Frank van Gilluwe, Second Edition, Addison-Wesley, 1997, ISBN 0-201-47950-8

7. APPENDIX B: DOCUMENT-REVISION HISTORY

Revision	Date	Edited by	Changes
ETX-CPU Specification.DOC	02/08/01	C. Cooper	Made global changes to replace j with #, updated drawings, applied new template, removed sections: LCD LVDS interface, serial ports, IRDA, parallel port, FDC, IDE, & audio specification.
ETX Specification	02/22/01	C. Cooper	Changed document title to ETX Component SBC. Updated signal names. Removed Electrical Characteristic chapter.
ETX Specification	03/01/01	R. Van Scoy S. Milnor	Revised some signal descriptions, added thermal management information and general editing to simplify text.
ETX Specification V2.5	3/22/01	B. Boyer	Formatting changes.
ETX Specification V2.6	5/09/01	R. Van Scoy	Revised pinout tables for X3 and X4, revised sections 4.3.2 and 4.3.3, added power management signal descriptions in 4.4.4.
ETX Specification V2.7	07/16/04	J. Lowell D. Gunter	Revised the following chapters: 3.3.2 (removed # after BUSY for Pin 86 BUSY entry in Parallel Port Mode Pinout table and deleted # sign from Pin 77 in Parallel-Port Mode Pinout and Floppy-Support Mode Pinout tables) 3.4 (added # to Pin 9 KBINH, Pin 10 LILED#, Pin 12 ACTLED#, and Pin 14 SPEEDLED# in Connector X4 table) 4.1.1 (changed wording in PCI Signals [General]) 4.3.2 (changed wording in JILI_CLK, JILI_DAT) 4.3.8 (removed # from BUSY entry in signal-description section) 4.4.2 (added # to Pin 10 LILED#, Pin 12 ACTLED#, and Pin 14 SPEEDLED# in signal-description section) 4.4.5 (added text to GPCS# signal description) 5.1 (changed mounting-hole and location-peg dimensions in Dimensions of ETX Component SBC drawing) 5.3 (changed table headings) 5.3.2 (deleted “Dimensions of Receptacle FX8-100S” drawing, changed location-peg dimensions and added outside dimensions in “PCB Footprint” drawing) 5.4 (changed mounting-hole and location-peg dimensions in “Backplane Layout” drawing. Editing and formatting changes throughout manual.
ETX Specifiaction V2.8	03/01/2006	Monica Ciolacu	Changed Corporate Offices and Web Addresses